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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,938	01/26/2004	Mohammed A. Fathimulla	P02,0004 01 H0002270 DIV	9312
128	7590 11/22/2006		EXAMINER	
HONEYWELL INTERNATIONAL INC.			PHAM, LONG	
P O BOX 22	MBIA ROAD 245	•	ART UNIT	PAPER NUMBER
	OWN, NJ 07962-2245		2814	
			DATE MAILED: 11/22/200	6

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/764,938	FATHIMULLA ET AL.				
Office Action Summary	Examiner	Art Unit				
	Long Pham	2814				
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet wit	h the correspondence address				
A SHORTENED STATUTORY PERIOD FOR REF WHICHEVER IS LONGER, FROM THE MAILING - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period. - Failure to reply within the set or extended period for reply will, by stat Any reply received by the Office later than three months after the material patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNIC 1.136(a). In no event, however, may a re- pot will apply and will expire SIX (6) MON tute, cause the application to become AB.	CATION. ply be timely filed THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 10	/16/06	•				
·	nis action is non-final.					
3) Since this application is in condition for allow		ers, prosecution as to the merits is				
closed in accordance with the practice unde	·	•				
	. Dr. parto Quayro, 1000 012	.,				
Disposition of Claims						
4)⊠ Claim(s) <u>1-6 and 22-35</u> is/are pending in the	application.					
4a) Of the above claim(s) 22-31 is/are withdr	awn from consideration.					
5) Claim(s) is/are allowed.	Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>1-6 and 32-35</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and	I/or election requirement.					
Application Papers						
9) The specification is objected to by the Exami	ner.					
10) The drawing(s) filed on is/are: a) a		ov the Examiner.				
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the corre						
11) The oath or declaration is objected to by the	• • • • • • • • • • • • • • • • • • • •					
Priority under 35 U.S.C. § 119		•				
12) Acknowledgment is made of a claim for foreign	an priority under 35 H S C &	119(a)-(d) or (f)				
a) All b) Some * c) None of:	gri priority under 55 0.0.0. g	113(4)-(4) 51 (1).				
1.☐ Certified copies of the priority docume	ents have been received					
2. Certified copies of the priority docume		polication No				
3. Copies of the certified copies of the pr	·	•				
application from the International Bure	•	The state of the s				
* See the attached detailed Office action for a li		received				
	•					
Attachment(s)						
1) Notice of References Cited (PTO-892)		ummary (PTO-413)				
2) Notice of Draftsperson's Patent Drawing Review (PTO-948))/Mail Date formal Patent Application				
Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	6) Other:					

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (US pat 5,438,220).

With respect to claim 1, Nakagawa et al. teach a semiconductor device comprising (see fig. 18 and associated text):

A high resistivity polysilicon handle wafer or polycrystalline layer 234;

A buried oxide layer 2 located directly on the polysilicon handle wafer; and

A silicon layer 4 located directly on the buried oxide layer.

Claims 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (US pat 5,438,220).

With respect to claim 1, Nakagawa et al. teach a semiconductor device comprising (see fig. 18 and associated text):

A high resistivity polysilicon handle wafer or polycrystalline layer 234;

A buried oxide layer 2 located directly on the polysilicon handle wafer or polycrystalline layer; and

A silicon layer 4 located directly on the buried oxide layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (US pat 5,438,220) as applied to claim 1 above, and further in view of the a pplicant's admitted prior art (AAPA) of this application and Temple et al. (US pat 4,905,075).

With respec to claim 2, Nakagawa et al. teach the wafer having high resistivity or updoped polysilicon but fail to teach that the device has an RF input.

AAPA teaches using high resistivity substrate or wafer to form RF device. See the Background of the Invention on pages 1 and 2 of this application.

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to include an RF input on the wafer of Nakagawa et al. to form an RF device having reduced losses and cross-talk. See the background of the Invention on pages 1 and 2 of this application.

With respect claim 32, Nakagawa et al. in combination with AAPA fail to teach that the polysilicon handle wafer has a resistivity of greater than 10⁶ ohmom.

Temple et al. teach using a polysilicon wafer or handle having a resistivity of greater than 10⁶ ohm-cm to provide a structure that can withstand mechanical shock. See col. 2, lines 1-5 and col. 5, lines 20-35.

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to incorporate the teaching of Temple et al. into the structure of Annamalai and AAPA to achieve the above benefit.

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With respect to claim 33, AAPA further teaches forming RF component in the silicon layer or wafer to reduce cross-talk.

Claims 5, 6, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (US pat 5,438,220) as applied to claims 3 and 4 above, and further in view of the a pplicant's admitted prior art (AAPA) of this application and Temple et al. (US pat 4,905,075).

With respec to claim 5, Nakagawa et al. teach the wafer having high resistivity or updoped polysilicon but fail to teach that the device has an RF input.

AAPA teaches using high resistivity substrate or wafer to form RF device. See the Background of the Invention on pages 1 and 2 of this application.

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to include an RF input on the wafer of Nakagawa et al. to form an RF device having reduced losses and cross-talk. See the background of the Invention on pages 1 and 2 of this application.

With respect to claim 6, Nakagawa et al. further teach the wafer is made of polysilicon or polycrystalline.

With respect claim 34, Nakagawa et al. in combination with AAPA fail to teach that the polysilicon handle wafer has a resistivity of greater than 10⁶ ohmom.

Temple et al. teach using a polysilicon wafer or handle having a resistivity of greater than 10⁶ ohm-cm to provide a structure that can withstand mechanical shock. See col. 2, lines 1-5 and col. 5, lines 20-35.

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to incorporate the teaching of Temple et al. into the structure of Annamalai and AAPA to achieve the above benefit.

With respect to claim 35, AAPA further teaches forming RF component in the silicon layer or wafer to reduce cross-talk.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham

Primary Examiner

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